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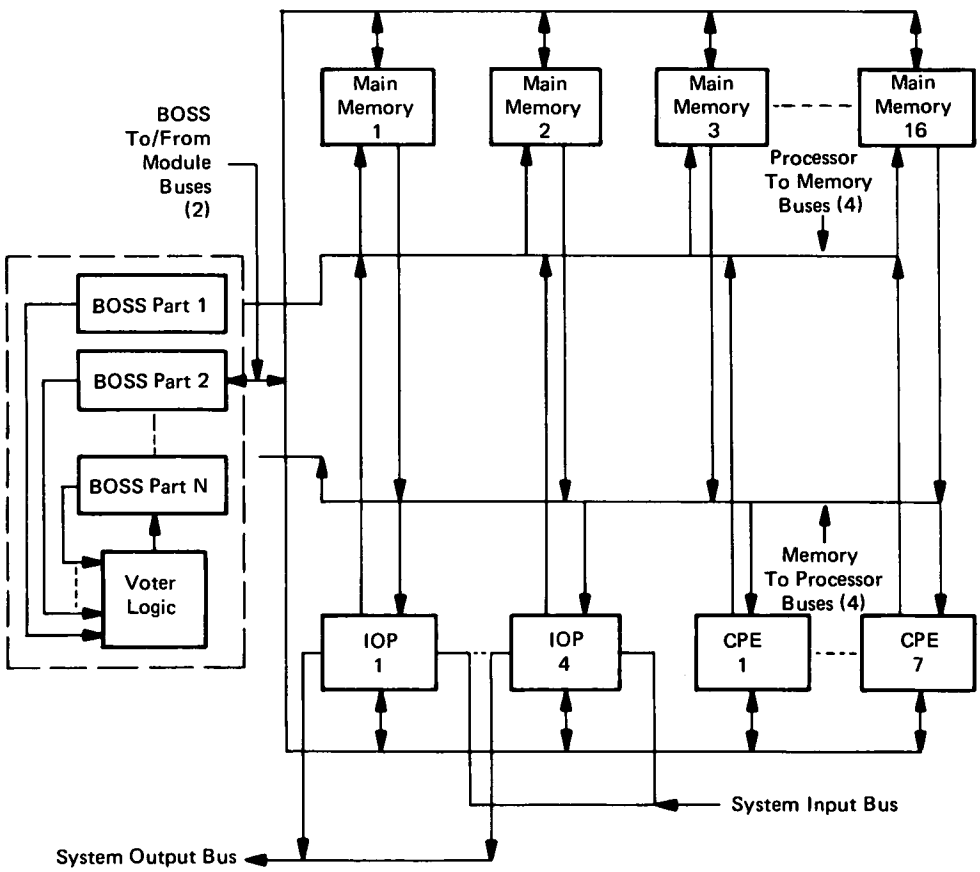
NASA TECH BRIEF

Marshall Space Flight Center

Modular Digital Computer System Design

A modular digital computer system, ARMMS (Automatically-Reconfigurable Modular Multiprocessor System), has been designed to provide redundant processing or multiprocessing with dynamic mode switching in real time. Because both modes are combined with dynamic switching in one computer, the same hardware is utilized for reliability enhancement, speed enhancement, or a combination of both. This is accomplished at a reasonable cost in system power, size, and complexity.

The ARMMS consists of a grouping of central processor elements (CPE's), I/O processors (IOP's), memory modules, and block organizer and system scheduler (BOSS) that will execute the following software routines: (a) data and I/O scheduling; (b) interrupt processing; (c) system test, repair, and configuration; and (d) power-and-clock switching and distribution. The IOP's, the CPE's, and the BOSS are connected to the memory modules by four pairs of buses, as shown in the figure.



ARMMS Configuration

(continued overleaf)

As a part of the design, an intermodule interface allows any CPE, IOP, or BOSS module to address any nonprotected memory page. It allows any combination of simplex, duplex, or TMR (triple modulator redundancy) streams with any combination of relative priorities to coexist with minimum bus contention, providing that no more than four CPE's, four IOP's, and a BOSS are involved simultaneously. Volatile storage defining a module role in the ARMMS has been minimized and can be coded so that transients cannot cause an undetected change in the module status. The interface allows all modules of a class (CPE, Memory, and the like) to be virtually identical. Interface gate complexity and module-to-module interconnections have been minimized.

Whenever a stream is formed, the BOSS sends each processor module involved a stream status code, defining all bus connections within the stream, and priority for that stream. Once assigned to a stream, a processor always uses the pair of buses specified by the stream status code for communication to and from memory, eliminating bus contention among processors of a given type. For redundancy, each processor can output on a choice of two buses, the choice being made by BOSS command.

To reduce bus contention between processors of different types, a hierarchy is established such that I/O and BOSS modules can inhibit CPE modules from starting a new memory access cycle, when the former modules require access to a memory bus. Similarly, BOSS (but not CPE) modules can inhibit bus access of I/O modules. Once any module has been granted access, it will continue to have it until transfer of the word involved has been completed. Usually only processors using buses needed by other processors are inhibited, except all processors operating synchronously in a duplex or a TMR stream are inhibited, if one or more processors in the stream are inhibited ensuring maintenance or synchronization between these processors. Modeling indicates that speed lost due to bus contention between processors of different types should be less than 3 percent, exclusive of memory contention losses that are independent of the interface design.

The ARMMS priority structure involves both hardware and software elements. The hardware recognizes a minimum of 16 different priority levels. The software then selects different subsets of these 16 as program requirements dictate. The highest hardware priority goes to the BOSS, since the efficiency of the rest of the system depends on the BOSS completing its tasks. The second highest priority is a special TMR, CPE mode used only in the event of an error in one of three TMR channels to ensure completion of the TMR task with maximum speed, prior to initiating diagnostic tests on the stream.

The next seven priorities are for I/O streams, on the assumption that the timing of external events happening and mass data transfers is more difficult to control than the timing within processing streams and, hence, that IOP memory access requests should be given higher priorities than CPE access requests. The seven lowest priorities are for CPE's. Different numbers of arrangements of priorities could be implemented easily if required.

Notes:

1. The new design will provide higher computer capability than that presently available for the same amount of hardware. It will furnish a modular system which is responsive to diverse problems effectively.
2. Requests for further information may be directed to:
   Technology Utilization Officer
   Marshall Space Flight Center
   Code A&PS-TU
   Marshall Space Flight Center, Alabama 35812
   Reference: B74-10034

Patent status:

Inquiries concerning rights for the commercial use of this invention should be addressed to:

Patent Counsel
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